Embedded Vision Architecture

Bottlenecks and Tradeoffs in High Frame Rate Visual Servoing: A Case Study

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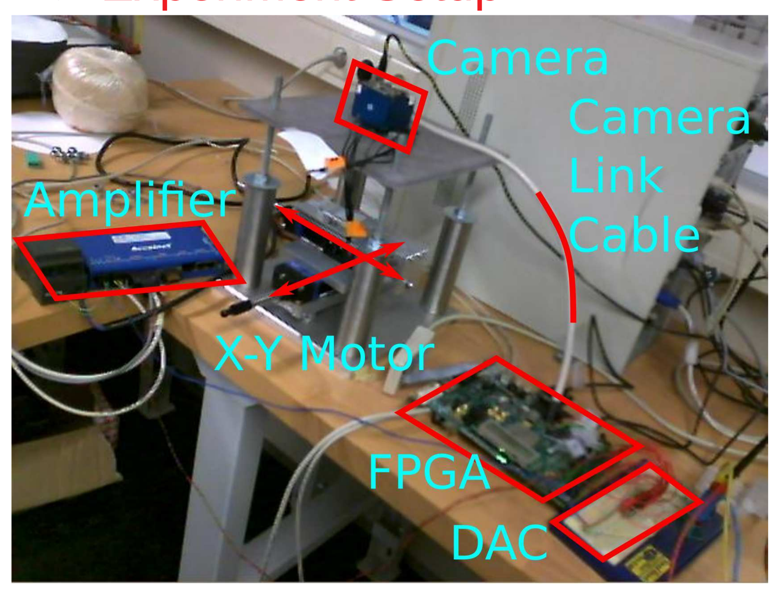
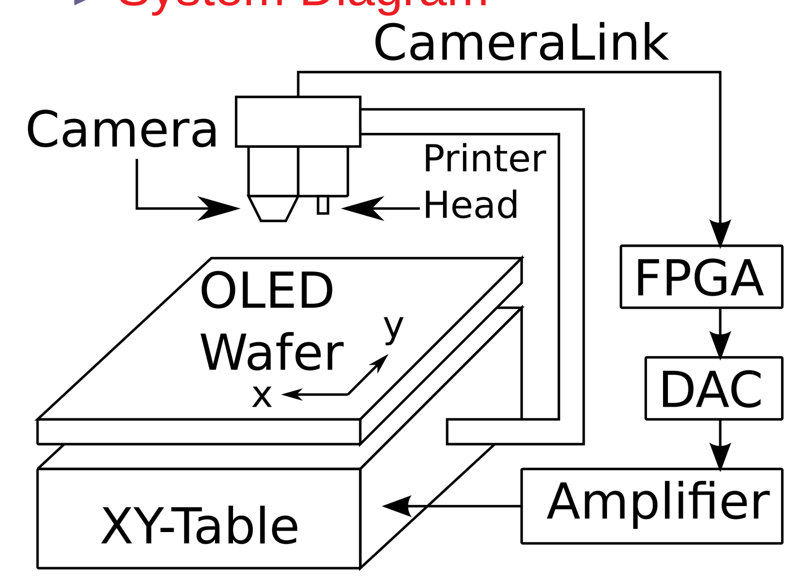
Case Study: Visual Servoing on Repetitive Structures

- Application: vision-based inkjet printing for OLED display manufacturing.
- Control Goal: printer head shoots chemical droplets on pixel centers.
- Mechanical Design: fixed camera and printer head, moving OLED wafer.
- Vision Processing: detecting centers of pixels on the OLED wafer.
- Control Algorithm: open-loop tracking or closed-loop trajectory generation.

- Experiment Setup



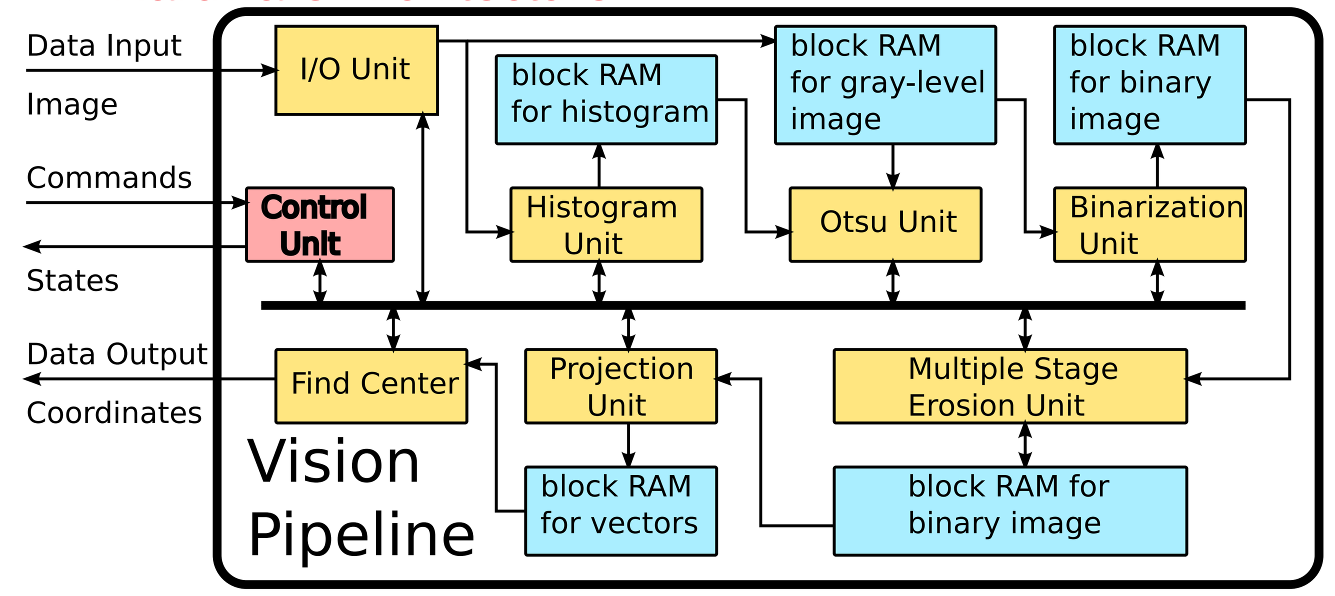
- System Diagram



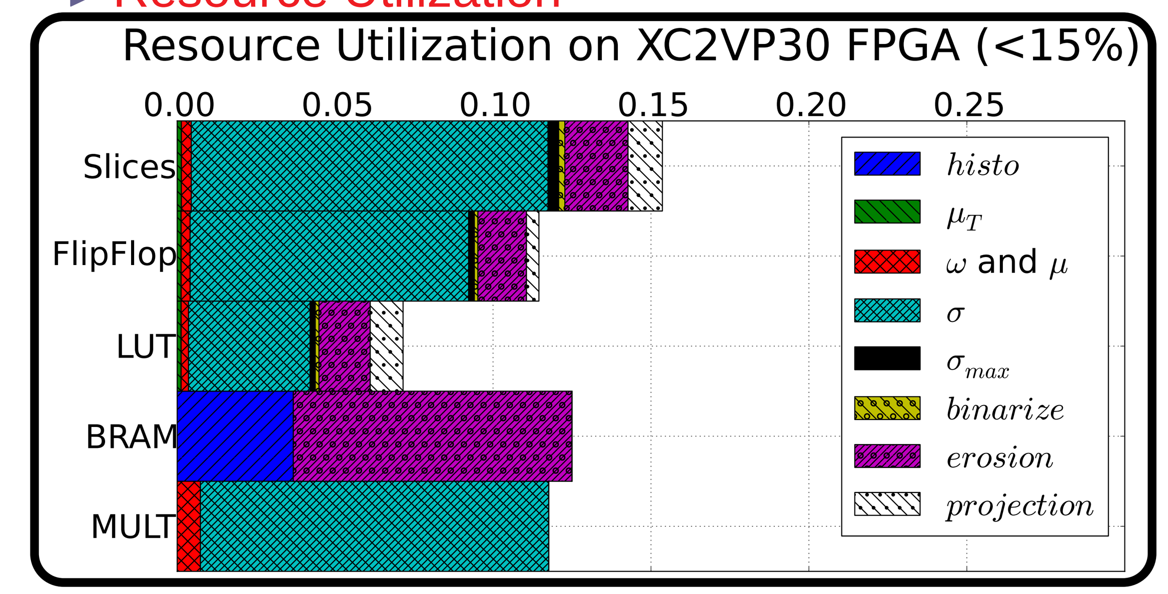
1000 Frames-per-Second (fps) Vision on FPGA – Hardware Architecture, Resource Utilization, and Timing Analysis

- Hardware Architecture: dedicated module for each pipeline stage, runs as a synchronous systolic array.
- Resource Utilization: this implementation is optimized for resource usage instead of performance, but it can scale to higher performance with more resource usage.
- Timing Analysis: concurrent tasks are executed in parallel with fine-grained pixel streaming.

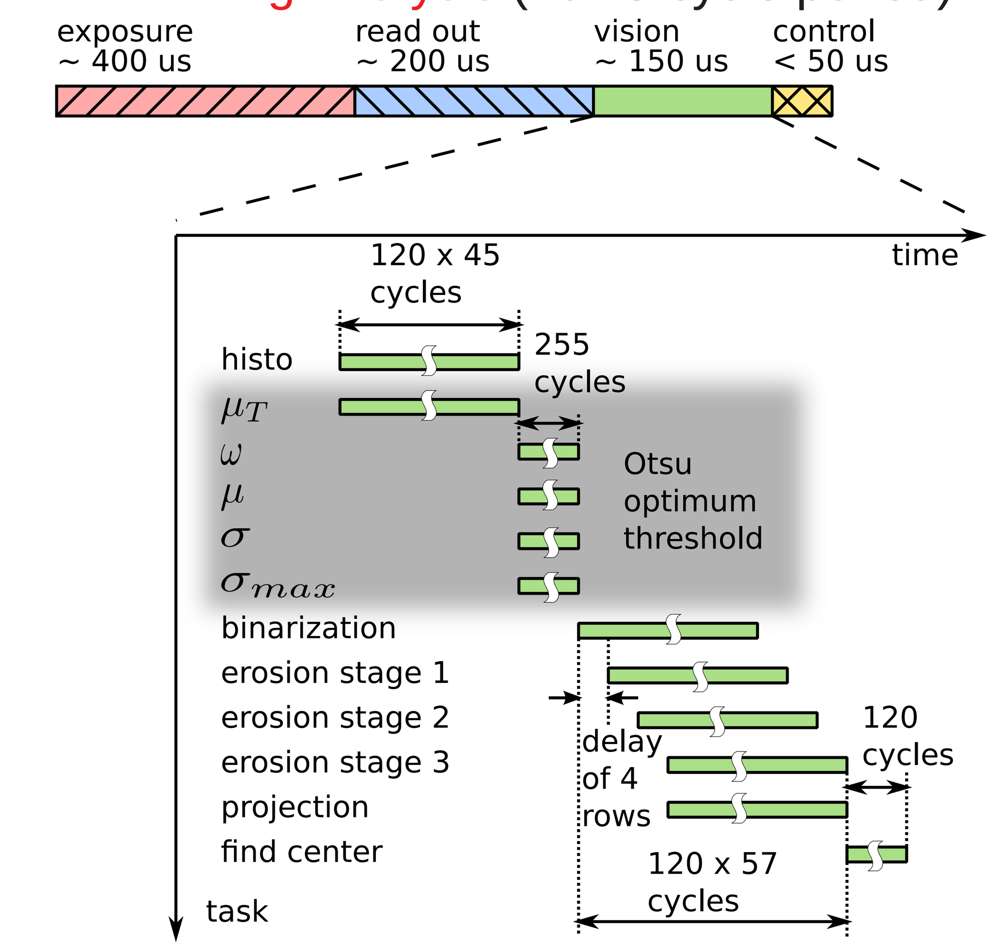
- Hardware Architecture



- Resource Utilization



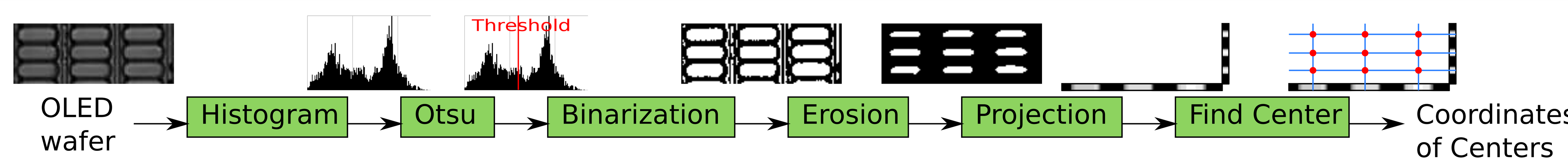
- Timing Analysis (10 *ns* cycle period)



Vision Pipeline For Detecting Pixel Centers of OLED Wafer Using a Small Region-Of-Interest (ROI)

Image Properties:

- Exposure: 400 μs under strong lighting
- Region-Of-Interest: 120×45 pixels
- Quantization: 8-bit gray scale

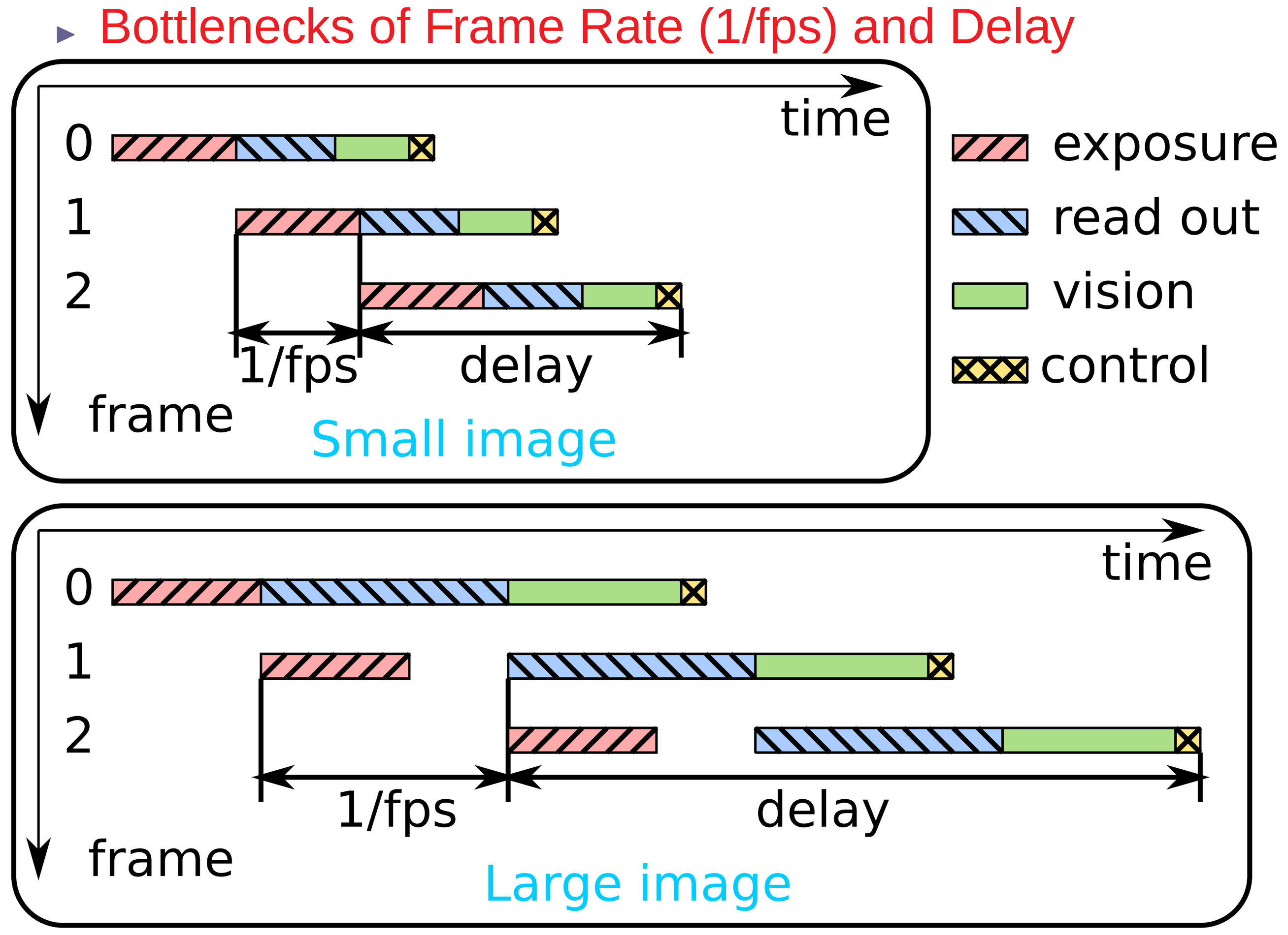


Major Algorithms:

- Otsu optimum thresholding to handle lighting variation
- Erosion for noise removal
- Projection of segmented features for fast center localization

Bottleneck Analysis – The Diminishing Return of Faster Vision Processing

- Bottlenecks of Frame Rate (1/fps) and Delay



Analysis Cases

- Industrial Camera: SVS-VISTEK svs340MUCP.
- Camera Interface: CameraLink.
- Processing System: Xilinx Virtex-II FPGA.

Without lost of generality, we also apply the same analysis to variant types of industrial cameras, camera interfaces, and FPGA-based processing systems. We found similar scaling.

Key Observations

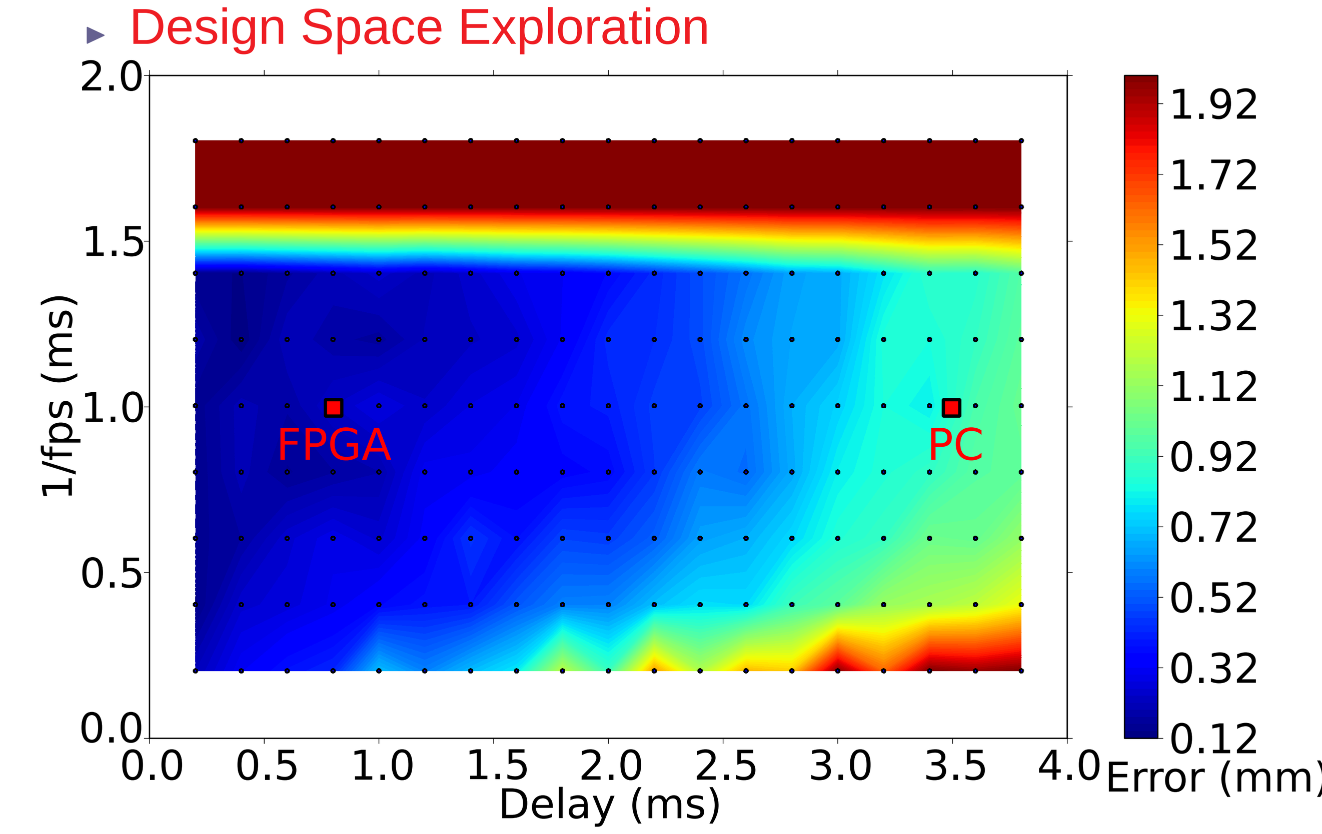
- Frame rate, for small image, is limited by exposure time
- Frame rate, for large image, is limited by image read out
- Delay is dominated by exposure and read out
- Vision processing on repetitive structures is neither the bottleneck of frame rate nor the bottleneck of delay

Future Trend

- Vision processing scales well with parallel hardware.
- An enlarging gap between industrial standard camera interface and vision processing.
- The diminishing return of faster vision processing.

Understanding The Tradeoffs: Frame Rate (1/fps), Delay and Control Performance

- Design Space Exploration



Simulating The Design Space

- Control Task: tracking the pixel centers of the moving wafer.
- Control Performance: measured as the maximum tracking errors of the pixel centers.
- Tracking Algorithm: linear predictor, tuned at 1000 fps.

Without lost of generality, we simulate different motion profiles. We found similar tradeoffs.

Key Observations

At high frame rate (above 1000 fps),

- The control performance is more sensitive on delay other than frame rate.
- Delay, not frame rate, gives embedded solution most advantage over PC solution.

Future Work

- A Cyber-Physical System Approach to Embedded Visual Servoing