

# ZHENYU YE

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## SUMMARY

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Commercial product development, from prototyping to mass production. Wireless and low-power Internet-of-things devices at industrial scale. Optimisation of computer vision and machine learning algorithms on custom hardware. Implementation of electronics systems, from chip design to firmware/software stack. Integration of electronics systems into mechatronics and robotics systems.

## PROFESSIONAL EXPERIENCE

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### **Hardware and Devices Engineer, Connecterra**

*2016 July - current*

- ◊ Commercial product development, from prototyping to mass production.
  - ◊ Electronics, firmware, and software for wireless Internet-of-things devices.
  - ◊ Optimisation of machine learning algorithms on battery-powered devices.
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### **Firmware Engineer, Intel**

*2014 August - 2016 June*

Implementation of firmware for next generation image signal processors. Major activities:

- Implementation of firmware stack for customized circuits and signal processors.
  - Support Windows and Android driver teams for bringing up and troubleshooting device features.
  - Interact with image algorithm designers for implementation and interface of firmware.
  - Practice software design process and agile development method.
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### **Guest lecturing on visual computing on GPUs, TU Eindhoven**

*2009 - 2016*

- ◊ Giving lectures on GPU architectures and programming for a master level course.
  - ◊ Assisting hands-on labs on the implementation and optimization of various image and vision algorithms on GPUs: histogram equalization (2009), stereo vision (2010), natural feature detection (2011), face detection (2012), and neural networks for object recognition (2013).
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### **Researcher, Embedded vision, TU Delft**

*2014 April - July*

Implementation and optimization of a proprietary computer vision algorithm on parallel processing platforms. The project later turns into a startup, QdepQ.

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### **PhD researcher, Embedded vision architecture, TU Eindhoven**

*2009 - 2014*

- ◊ Design of vision algorithms and electronic systems for 1000 frames-per-second vision processing.
- ◊ Implementation of vision based closed-loop control systems, a.k.a. "vision-in-the-loop" systems, for precision motion control (see my homepage for a demo).
- ◊ Cooperation with multiple industrial partners and a multidisciplinary team.

Major achievements:

- High-speed vision processing on field-programmable gate arrays (FPGAs).
- Implementation of micro-/nano-scale visual servo control systems.
- Multi-domain modeling of data-intensive and compute-intensive mechatronic systems.

Relevant knowledge and skills:

- **Electronic systems:** parallel architecture, register-transfer level (RTL) design using hardware description languages (e.g., VHDL/Verilog), high-level-synthesis tools (various vendors), FPGA tool-chains (various vendors), high-speed interfaces for image sensors and cameras (e.g., LVDS, CameraLink).
  - **Embedded software:** C/C++ targeting various embedded processors (e.g., DSP, Microblaze), single-instruction-multiple-data (SIMD) extensions (e.g., Intel SSE), programming graphics processing units (GPUs) with CUDA and OpenCL, multi-threading on multi-core processors (e.g., pthread, OpenMP), real-time operating systems (e.g., Real-Time Linux), scripts (e.g., Python).
  - **Image processing:** design of hardware-friendly image processing algorithms from scratch and from existing libraries (e.g., Matlab, OpenCV), image processing on CPU/DSP/GPUs/FPGAs, full-system implementation of high-speed (1000 fps) imaging platform.
  - **Mechatronics systems:** digital and analog interface (e.g., various ADC/DAC), motor encoder and actuator interface, design of feedforward and feedback controllers, modeling and simulation (e.g., in Matlab/Simulink), performance tuning for measurement noise and delay of visual feedback.
  - **Modeling, simulation, analysis:** analytical performance model of image processing systems, quality analysis of vision algorithms for control purposes, multi-domain modeling and integration, customized full-system simulation framework, system-wide bottleneck analysis and optimization.
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**Team member, Low-power image processor architecture, TU Eindhoven** *2009 - 2013*

Relevant knowledge and skills:

- **Processor architecture:** micro-architecture of processors (RISC/VLIW/SIMD), memory hierarchy optimization (e.g., configuration of register file and memory).
  - **Embedded software:** assembly code level optimization on SIMD architecture.
  - **Image processing:** design and implementation of hardware-friendly image processing algorithms.
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**MSc project, GPU architecture and programming, TU Eindhoven** *2008 - 2009*

Relevant knowledge and skills:

- **GPU programming:** general purpose computing in CUDA, graphics pipeline in OpenGL.
  - **Parallel computing:** parallel implementation of linear algebra algorithms (BLAS/LAPACK).
  - **Modeling & simulation:** analytical models, simulators (e.g., SimpleScalar, GPGPU-Sim).
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## EDUCATION

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**PhD candidate, TU Eindhoven, The Netherlands** *2009 - 2017 (expected)*

Funded by the Embedded Vision Architecture project, in cooperation with the Dynamics & Control group and the Electronic Systems group of TU Eindhoven, and the Biorobotics Lab of TU Delft.

**MSc. (Ir.) in Embedded Systems, TU Eindhoven, The Netherlands** *2006 - 2009*

Funded by TU/e scholarship, with MSc. thesis on GPU architecture and programming.

**BSc., Electronic Engineering, Harbin Institute of Technology, China** *2002 - 2006*

BSc. project on the implementation and optimization of digital filters on DSPs.

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## ADDITIONAL INFORMATION

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**Personal info:** Nationality: P.R.China, Date of Birth: 16 Oct. 1983, Gender: Male

**Language skills:** English, Chinese, Dutch (A2-level, genoeg voor koetjes-en-kalfjes)